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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,512	06/30/2000	Reynold V. D'Sa	2207/P6786	9566

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/608,512	D'SA ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-13* is/are allowed.

6)☒ Claim(s) *1-6 and 14-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

2. The oath or declaration filed on September 11, 2000 is defective because: Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Inoue, US Patent 6,851,043 (herein referred to as Inoue).

6. Referring to claim 14, Inoue has taught a method comprising:

a. writing at least one micro-op into a decoded micro-op cache (column 8, lines 8-12);

b. retiring the at least one instruction (column 22, lines 25-33); and

c. removing entries from a branch prediction logic storage buffer that would later produce bogus branches (The BRHIS is interpreted to be the claimed buffer. Entries in the BRHIS are updated such that history entries that would later produce bogus branches are removed. Specifically see column 17, lines 4-18, also see Figure 3, column 2, lines 22-47, column 8, line 29-column 10, line 43, column 14, line 66-column 15, line 25, column 15, line 62-column 16, line 7, column 32, lines 59-65, column 33, lines 6-13, column 35, lines 48-67, column 36, line 53-60, column 37, lines 9-16, column 38, lines 32-38).

7. Referring to claim 15, Inoue has taught the apparatus according to claim 14, as described above, and wherein retiring the at least one micro-op comprises at least:

a. determining what the actual result for the retired at least one micro-op was (column 12, lines 65-67).

8. Referring to claim 16, Inoue has taught the apparatus of claim 14, as described above, and wherein scrubbing the branch prediction logic storage buffer comprises at least:

a. comparing what an actual result of the retired at least one micro-op is to an instruction trace in the branch prediction logic storage buffer (column 12, lines 65-67, column 14, lines 41-65).

9. Referring to claim 17, Inoue has taught the method according to claim 14, as described above, and wherein scrubbing the branch prediction logic storage buffer further comprises at least one of:

a. deallocating any other micro-ops pertaining to the at least one retired micro-op;

b. deallocating at least one old set which had been overwritten in the decoded micro-op cache by a built instruction "trace";

c. deallocating at least one entry that is related to a branch in at least one old set in the decoded micro-op cache; and

d. deallocating at least one entry that is related to a branch of at least one old set in the decoded micro-op cache that is downstream from the at least one retired micro-op (column 15, line 62-column 16, line 7, Figure 3, column 2, lines 22-47, column 8, line 29-column 10, line 43, column 14, line 66-column 15, line 25, column 15, line 62-column 16, line 7, column 32, lines 59-65, column 33, lines 6-13, column 35, lines 48-67, column 36, line 53-60, column 37, lines 9-16, column 38, lines 32-38, instructions following a phantom branch or a branch with an invalid target address are invalidated and deleted from being committed.).

10. Referring to claim 18, Inoue has taught the method according to claim 14, as described above, and wherein scrubbing can be accomplished at the time of at least one of writing or retiring (column 12, lines 65-67, column 14).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1-6 and 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue, US Patent 6,851,043 (herein referred to as Inoue), in view of McCrocklin et al., US Patent 4,761,733 (herein referred to as McCrocklin).

13. Referring to claim 1, Inoue has taught a method comprising:

a. predicting by branch prediction logic whether the at least one micro-op is a branch (column 2, line 49-column 3, line 22);

b. executing the at least one micro-op (column 2, lines 49-67);

c. determining if the at least one executed micro-op is a bogus branch of the first macro instruction (column 2, line 48-column 3, line 22, column 5, lines 10-45, column 6, lines 15-29, column 7, line 54-column 8, line 8, column 8, lines 29-55, column 13, lines 1-27, column 14, lines 41-65, column 17, lines 3-18, column 29, lines 30-45, column 32, lines 34-43, column 33, lines 38-42, column 36, lines 40-60, column 36, line 63-column 37, line 15, column 38, lines 18-38, Determining whether an instruction contains a valid target address or determining whether an instruction is selected and determined to be a branch instruction, i.e. phantom branch (mistakenly predicting that a branch is selected)); and

d. continuing processing with a second macro instruction (column 2, lines 14-33, column 5, lines 21-45, column 6, lines 1-30, column 8, lines 2-column 9, line

7, column 32, lines 30-34 and 55-59, column 33, lines 1-5 and 38-42, column 36, lines 49-60, column 36, line 62-column 37, line 15, column 38, lines 27-38, Instructions following possible branch instructions are speculatively executed and flagged with bits, see figure 3.)

e. wherein if the at least one executed micro-op is determined to be a bogus branch, then the method further comprises:

i. flagging any other micro-ops which pertain to the at least one executed bogus branch micro-op (column 2, lines 14-33, column 5, lines 21-45, column 6, lines 1-30, column 8, lines 2-column 9, line 7, column 32, lines 30-34 and 55-59, column 33, lines 1-5 and 38-42, column 36, lines 49-60, column 36, line 62-column 37, line 15, column 38, lines 27-38, instructions following possible branch instructions are speculatively executed and flagged with bits, see figure 3.);

ii. removing the flagged micro-ops for retirement (Figure 3, column 2, lines 22-47., column 8, line 29-column 10, line 43, column 14, line 66-column 15, line 25, column 15, line 62-column 16, line 7, column 32, lines 59-65, column 33, lines 6-13, column 35, lines 48-67, column 36, line 53-60, column 37, lines 9-16, column 38, lines 32-38, instructions following a phantom branch or a branch with an invalid target address are invalidated and deleted from being committed.); and

iii. scrubbing a branch prediction logic storage buffer upon which the branch prediction logic is based (column 12, lines 65-67)

14. Inoue has not taught: decoding a first macro instruction into at least one micro-op; writing the at least one micro-op into a decoded micro-op cache. McCrocklin has taught:

a. decoding a first macro instruction into at least one micro-op (McCrocklin column 1 lines 23-33);

b. writing the at least one micro-op into a decoded micro-op cache (McCrocklin column 6 lines 49-61, column 7 lines 25-49);

15. It would have been obvious to one of ordinary skill in the art at the time of the invention to use microinstruction processors because modern computer systems typically include a micro-programmable microprocessor, which will utilize macroinstructions and microinstructions (McCrocklin column 1 lines 9-33). Since this is a typical embodiment for microprocessors, as shown by McCrocklin, one of ordinary skill in the art would have recognized the benefit in using microinstructions and macroinstructions, where the tasks are broken down into more basic functions which can be executed faster than one complex instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a microprocessor with microinstructions to speed up the execution of the instructions.

16. Referring to claim 2, Inoue and McCrocklin have taught the method according to claim 1, as described above, and further comprising: fetching from a main memory the macro instruction (McCrocklin column 1 lines 23-33).

17. Referring to claim 3, Inoue has taught the method according to claim 1, as described above, and wherein the at least one micro-op is written into the decoded

micro-op cache in an order a branch table buffer predicts that the at least one micro-op should be executed (column 15, line 47-column 16, line 7).

18. Referring to claim 4, Inoue has taught the method according to claim 1, as described above, and wherein executing the at least one micro-op is in at least one of an "in-order" or "out-of-order" fashion (column 15, line 47-column 16, line 7).

19. Referring to claim 5, Inoue has taught the method according to claim 1, as described above, and wherein scrubbing the branch prediction logic storage buffer further comprises at least one of:

a. deallocating any other micro-ops pertaining to the at least one executed bogus branch micro-op;

b. deallocating at least one old set which had been overwritten in the decoded micro-op cache by a built instruction "trace";

c. deallocating at least one entry that is related to a branch in at least one old set in the decoded micro-op cache; and

d. deallocating at least one entry that is related to a branch of at least one old set in the decoded micro-op cache that is downstream from the at least one executed bogus branch micro-op (Figure 3, column 2, lines 22-47., column 8, line 29-column 10, line 43, column 14, line 66-column 15, line 25, column 15, line 62-column 16, line 7, column 32, lines 59-65, column 33, lines 6-13, column 35, lines 48-67, column 36, line 53-60, column 37, lines 9-16, column 38, lines 32-38, instructions following a phantom branch or a branch with an invalid target address are invalidated and deleted from being committed.).

20. Referring to claim 6, Inoue has taught the method according to claim 1, as described above, and further comprising: determining if the branch has been taken (Figure 3, "taken" field).

21. Referring to claim 19, Inoue has taught an apparatus comprising:

a. a branch prediction logic storage buffer to predict whether a branch will be taken upon execution of the at least one decoded micro-op (column 17, lines 4-18, branch history table);

b. an instruction execution unit to execute the at least one micro-op (column 5, lines 21-33); and

c. an instruction retirement unit which is to determine whether the at least one micro-op is of a bogus branch macro instruction (column 2, line 48-column 3, line 22, column 5, lines 10-45, column 6, lines 15-29, column 7, line 54-column 8, line 8, column 8, lines 29-55, column 13, lines 1-27, column 14, lines 41-65, column 17, lines 3-18, column 29, lines 30-45, column 32, lines 34-43, column 33, lines 38-42, column 36, lines 40-60, column 36, line 63-column 37, line 15, column 38, lines 18-38. determining whether an instruction contains a valid target address or determining whether an instruction is selected and determined to be a branch instruction, i.e. phantom branch (mistakenly predicting that a branch is selected)),

d. wherein if the instruction retirement unit determines the at least one micro-op is of a bogus branch macro instruction, any other micro-ops stored in the decoded micro-op cache pertaining to that bogus branch macro instruction are

flagged and removed to the instruction retirement unit for retirement (Figure 3, column 2, lines 22-47., column 8, line 29-column 10, line 43, column 14, line 66-column 15, line 25, column 15, line 62-column 16, line 7, column 32, lines 59-65, column 33, lines 6-13, column 35, lines 48-67, column 36, line 53-60, column 37, lines 9-16, column 38, lines 32-38, instructions following a phantom branch or a branch with an invalid target address are invalidated and cleared from being committed.)

e. and the branch prediction logic storage buffer is scrubbed (column 12, lines 65-67, column 17, lines 5-18).

22. Inoue has not taught a decoded micro-op cache into which are written at least one decoded micro-op of a macro instruction. McCrocklin has taught a decoded micro-op cache into which are written at least one decoded micro-op of a macro instruction (McCrocklin column 1 lines 23-33, column 6 lines 49-61, column 7 lines 25-49). It would have been obvious to one of ordinary skill in the art at the time of the invention to use microinstruction processors because modern computer systems typically include a micro-programmable microprocessor, which will utilize macroinstructions and microinstructions (McCrocklin column 1 lines 9-33). Since this is a typical embodiment for microprocessors, as shown by McCrocklin, one of ordinary skill in the art would have recognized the benefit in using microinstructions and macroinstructions, where the tasks are broken down into more basic functions which can be executed faster than one complex instruction. Therefore, it would have been obvious to one of ordinary skill in the

art at the time of the invention to use a microprocessor with microinstructions to speed up the execution of the instructions.

23. Referring to claim 20, the combination of Inoue and McCrocklin have taught the apparatus of claim 19, as described above, and further comprising: a main memory in which the macro instruction is stored; and an instruction fetch unit for fetching the macro instruction from the main memory (McCrocklin column 1 lines 23-33).

24. Referring to claim 21, Inoue and McCrocklin have taught the apparatus of claim 19, as described above, and further comprising: an instruction decode unit for translating the macro instruction into the at least one decoded micro-op (McCrocklin column 1 lines 23-33; it is inherent that if the system decodes the macroinstructions into microinstructions that some decode unit must exist in the system).

25. Referring to claim 22, Inoue has taught the apparatus according to claim 19, as described above, and further comprising: a jump execution unit which determines whether a branch was taken upon execution of the at least one decoded micro-op (column 14, lines 8-15).

26. Referring to claim 23, Inoue has taught the apparatus according to claim 19, as described above, and wherein the branch prediction logic storage buffer applies branch prediction logic to predict whether a branch will be taken upon execution of the at least one decoded micro-op (column 7, lines 54-62).

27. Referring to claim 24, Inoue has taught the apparatus according to claim 19, as described above, and wherein if the branch prediction logic storage buffer predicts a

branch will be taken upon execution of the at least one decoded micro-op, an instruction trace is built pertaining to the predicted branch (column 17, lines 4-19).

28. Referring to claim 25, the combination of Inoue and McCrocklin have taught the apparatus of claim 24, as described above, and wherein the built instruction trace is inserted into the decoded micro-op cache such that the micro-ops of the branch macro-instruction are executed (Inoue and McCrocklin, the trace, or flags that Inoue uses to flag the instructions associated with a branch would be put on to the instruction still awaiting to be executed in the cache after being fetched based on the branch prediction).

29. Referring to claim 26, Inoue has taught the apparatus of claim 19, as described above, and wherein the branch prediction logic storage buffer is scrubbed by deallocation of at least one of any other micro-ops pertaining to the bogus branch macro instruction, any old set which had been overwritten in the decoded micro-op cache by a built instruction "trace", all entries that are related to any branches in the old set, and all entries that are related to the branches in the old set that are downstream from the retired branch macro instruction (column 12, lines 65-67).

Response to Arguments

30. Applicant's arguments filed December 22, 2006 have been fully considered but with respect to claims 1-6 and 14-25 they are not persuasive.

31. On page 10, Applicant argues with respect to claim 14 in essence:

> *"It is unclear where Inoue teaches a branch prediction logic storage buffer and where Inoue teaches removing entries."*

However, the BRHIS in Inoue is interpreted to be the claimed buffer. Entries in the BRHIS are updated such that history entries that would later produce bogus branches are removed and updated according to the entries of RSBR. Specifically see column 17, lines 4-18. RSBR entries are illustrated in Figure 3 and described at column 8, line 29-column 10, line 44. Also see the rejection above. Therefore this argument is moot.

32. On page 10, applicant argues with respect to claim 14 in essence:

"It also appears that the office action is citing to sections discussing non-selected branches, not bogus branches."

However, a bogus branch literally means "not a genuine branch". When Inoue mistakenly predicts that a branch is selected, this is interpreted as a bogus branch since the branch was not actually supposed to be selected and is not a genuine branch. So the selection of branches is pertinent to the interpretation of the claims to the reference and this is why discussions of non-selected branches were cited in the rejection. Therefore this argument is moot.

33. On page 11, Applicant argues with respect to claim 1 in essence:

"In Inoue, a phantom branch is being identified, but nothing is being done with any "other" branches that "pertain" to the phantom branch."

However, in claim 1 Applicant has not claimed anything about "other" branches that pertain to the phantom branch. Claim 1 merely states "flagging any other micro-ops which pertain to the at least one executed bogus branch micro-op". So the fact that Inoue may not do anything with other branches that pertain to the phantom branch is irrelevant since applicant has claimed flagging any "other"

micro-ops generically, where the micro-ops are not necessarily "other branches". Therefore this argument is moot.

Allowable Subject Matter

34. Claims 7-13 are allowed.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLM

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03/01/2007